

FIG. 1

A detailed cross-sectional view of a semiconductor device. The device consists of a substrate 10 with a top layer 81a. A central region contains a wafer 20. Below the wafer, there are two main processing regions, 41 and 42, separated by a central barrier 40. The regions 41 and 42 are further divided into sub-regions 51 and 52. A top layer 82 is shown above the wafer 20. A central channel 60 is formed through the substrate, with a top layer 61 and a bottom layer 62. A side channel 30 is also present. An RF matching box is connected to the top of the device, and an exhaust unit is connected to the bottom. A power supply P is connected to the top of the device. A cross-section 53 is indicated by a dashed line.

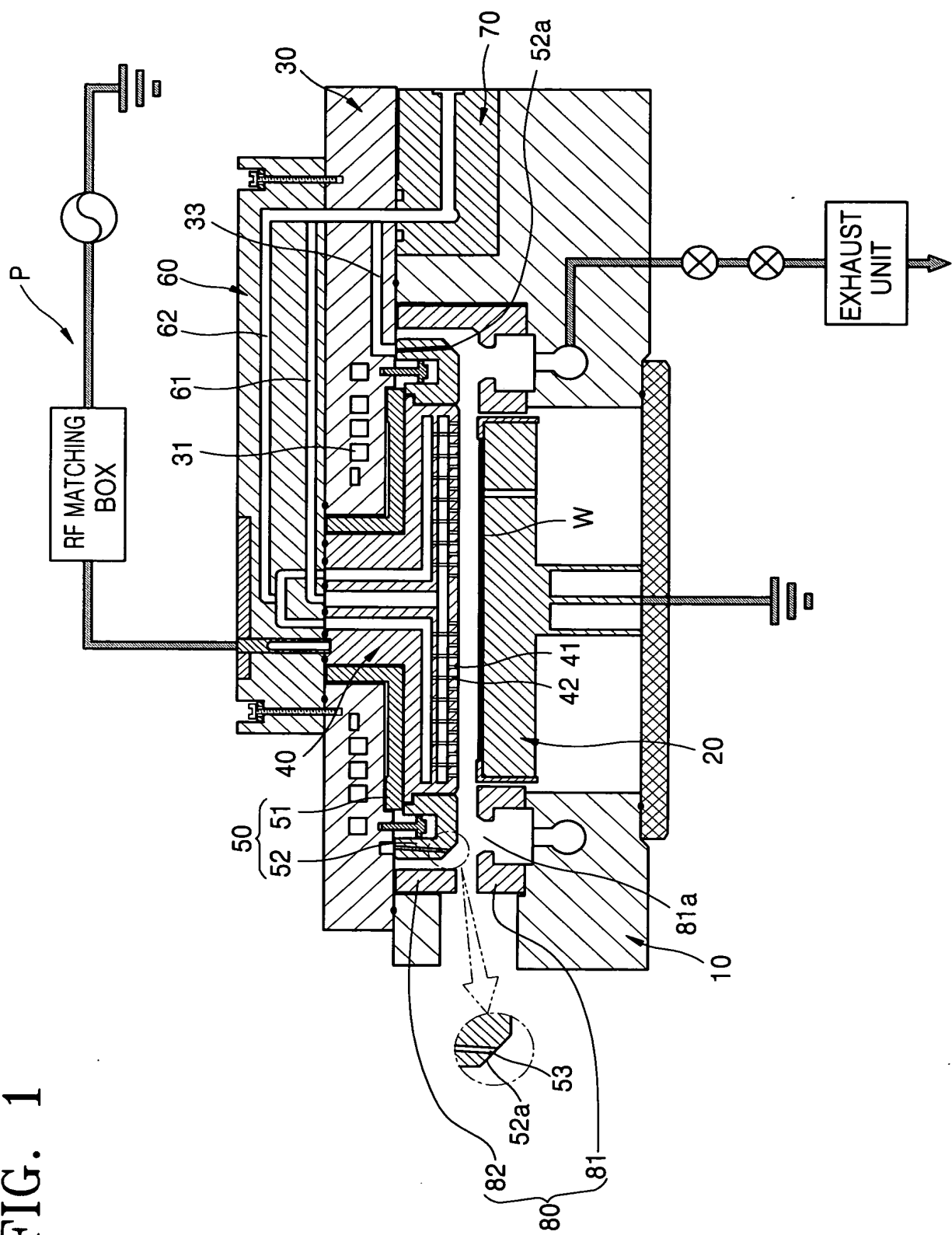


FIG. 2

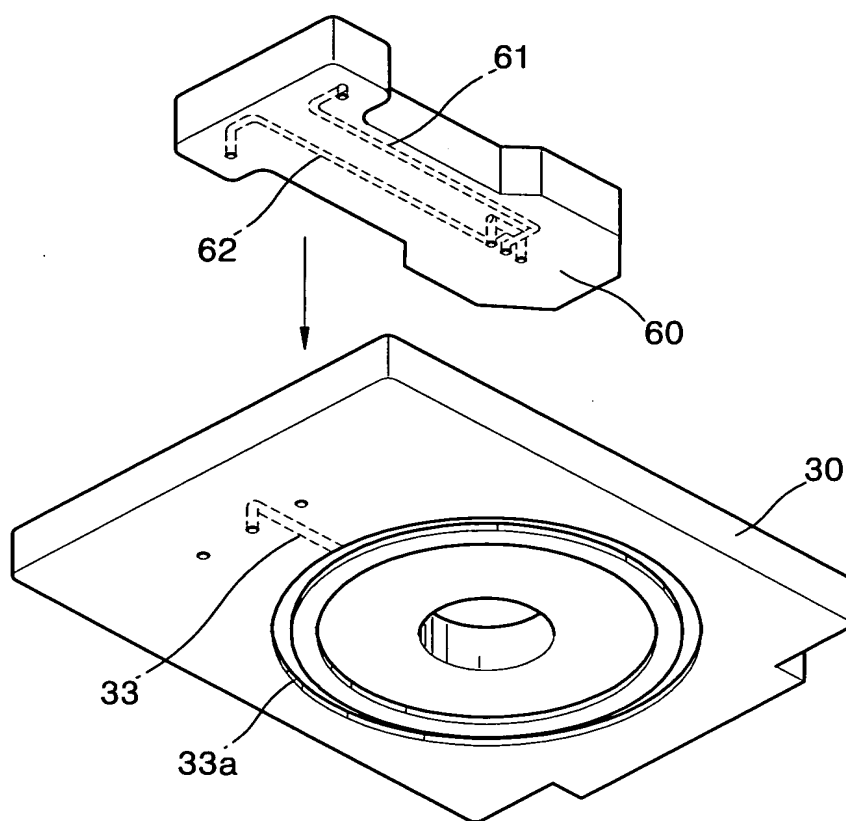


FIG. 3

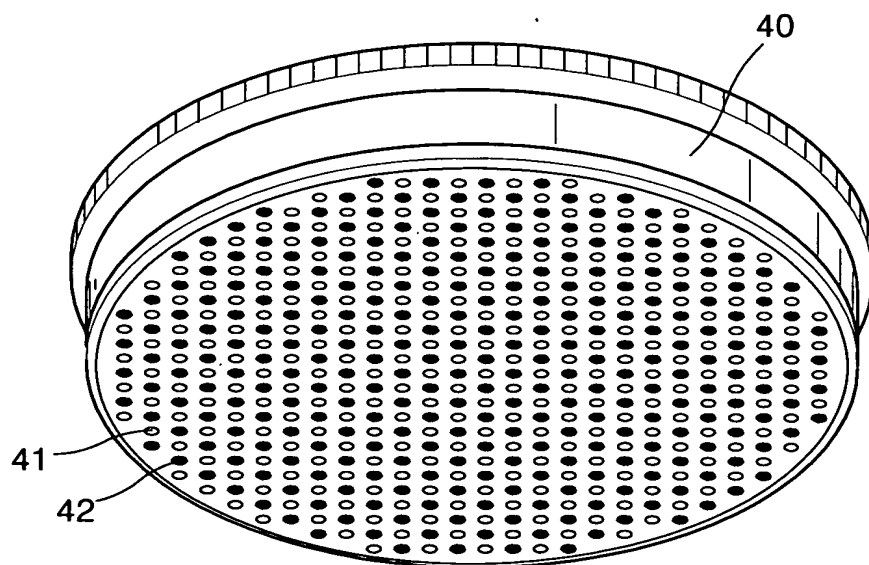


FIG. 4

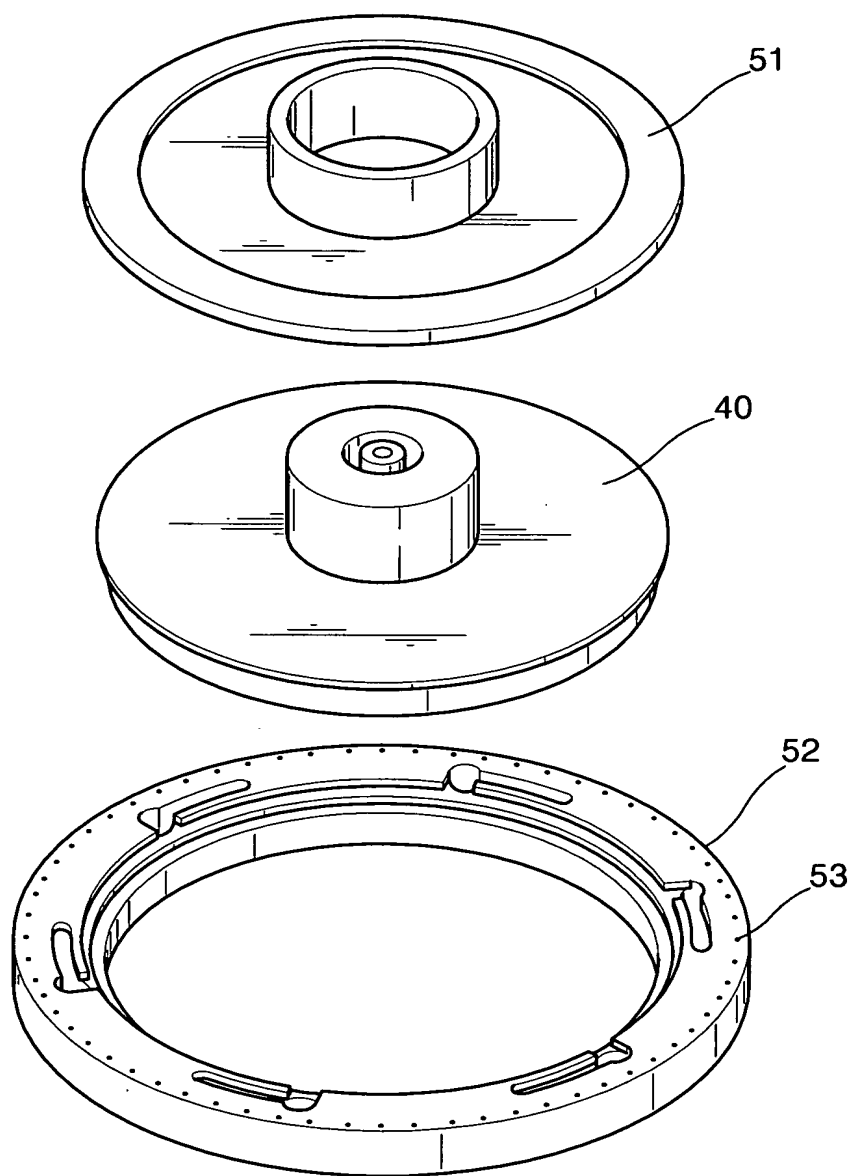
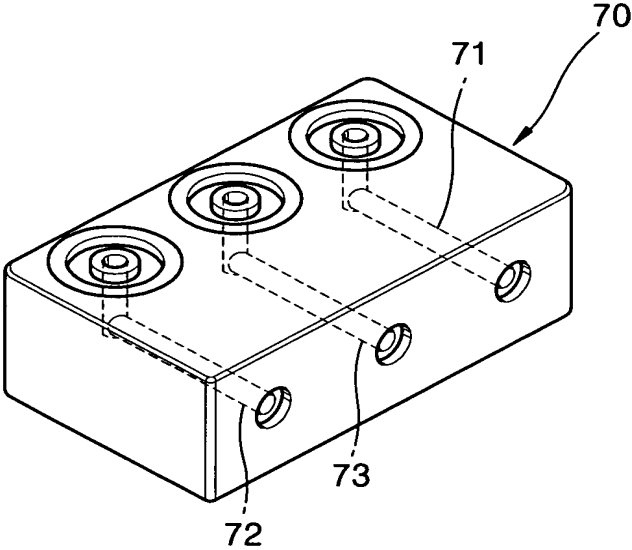


FIG. 5



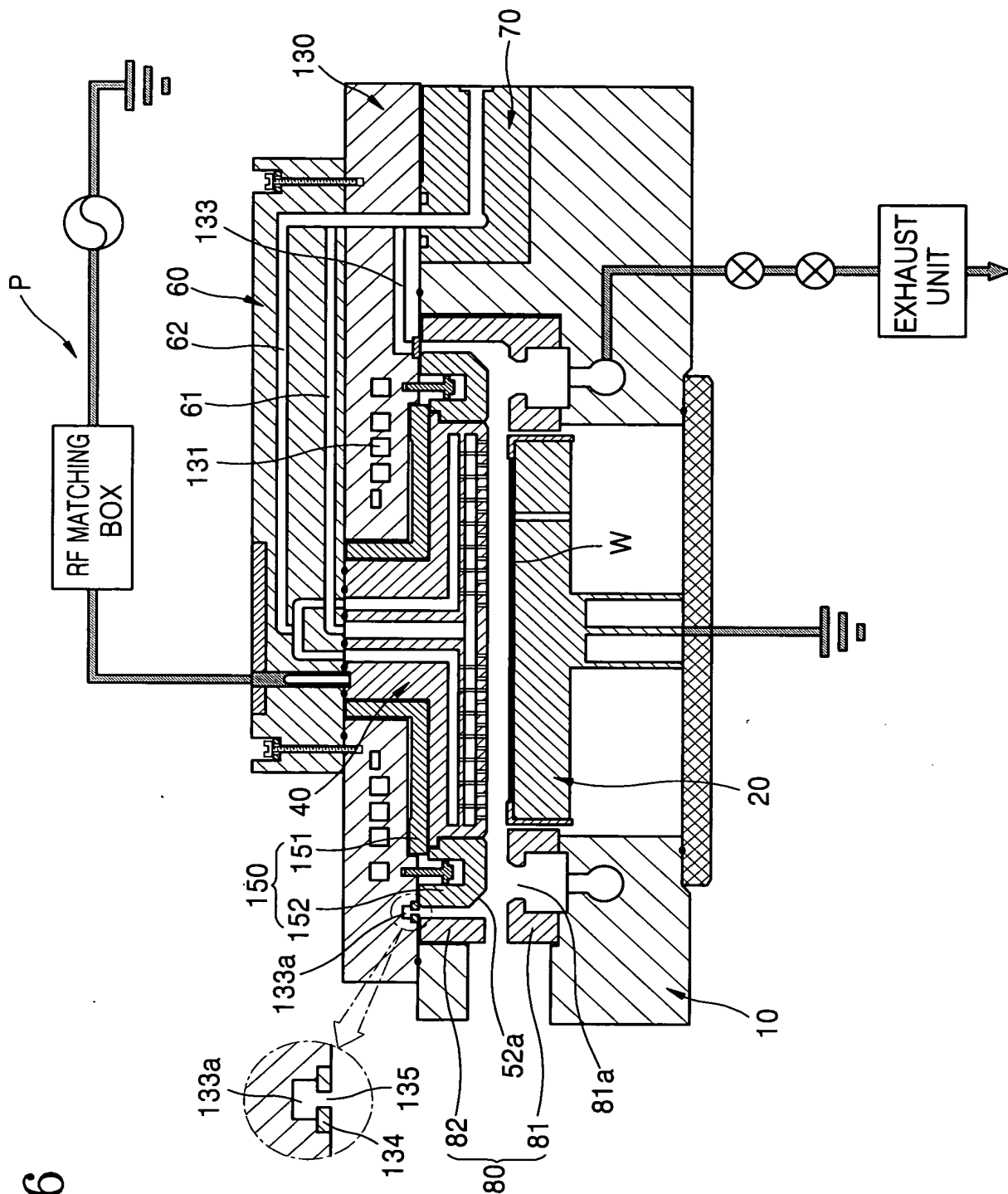


FIG. 7

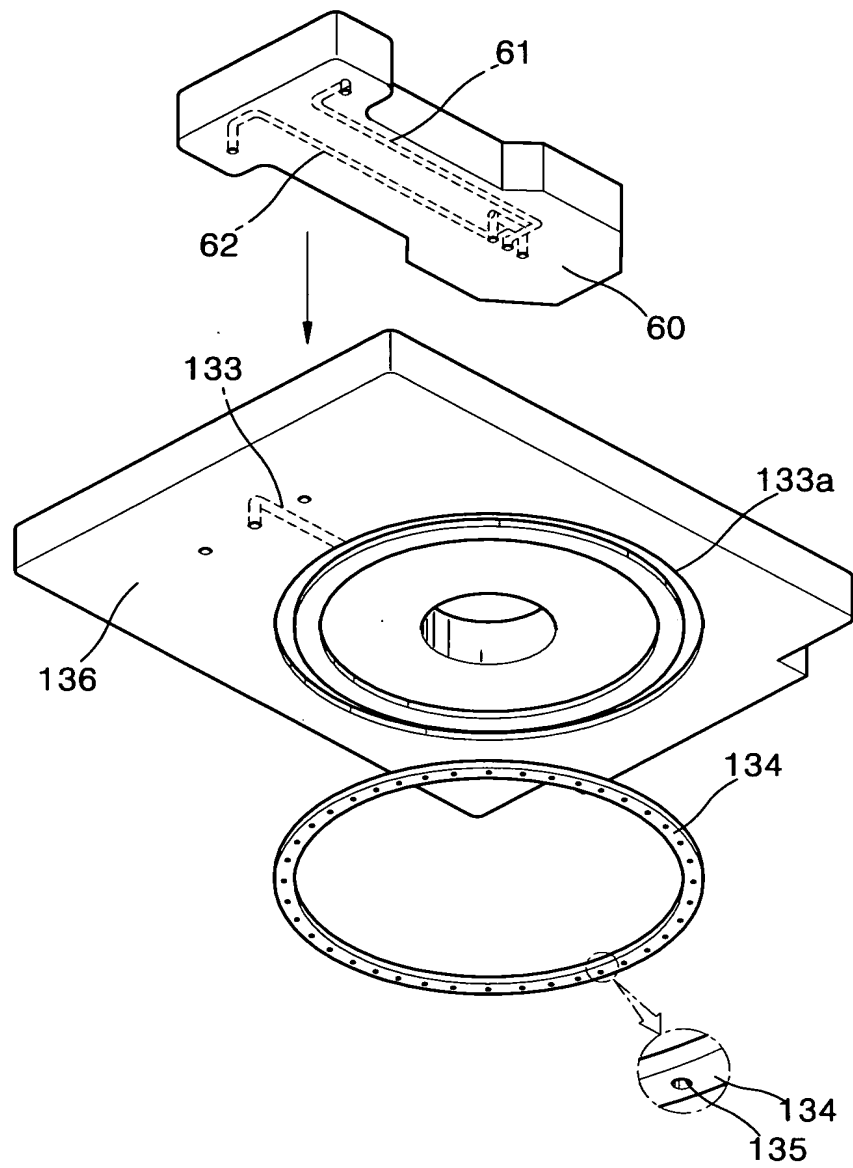


FIG. 8

